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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,181	05/08/2001	Theodore F. Vaida	01-035	2728

24319 7590 01/25/2005

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EXAMINER	
PHAN, TRI H	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,181	VAIDA ET AL.	
	Examiner	Art Unit	
	Tri H. Phan	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,9-11,13-17,19,23-25,27-31,33,37-39,41 and 42* is/are rejected.

7)☐ Claim(s) *4,6-8,12,18,20-22,26,32,34-36 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because all blocks in Figures 1-5 should be labeled with descriptive legends based on 37 C.F.R. § 1.84(o) for supporting the objection in the Rules and M.P.E.P. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 6, 15, 20-21 and 34-35 are objected to because of the following informalities:

In claim 6, line 4, "programable" in front of the term "logic core" is a typographical error; it should be correct to -- programmable --. Same objection's reasons with claim 20, line 3; claim 34, line 3.

In claim 15, line 9, the word "the" in front of the term "memory device" should be correct to -- a -- for clarity.

In claim 21, line 3, the word "the" in front of the term "support logic core" should be correct to -- to -- for clarity. Same objection's reason with claim 35, lines 3-4.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In regard to claim 2, line 2, the term "may be" is vague and indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention or not, and the resulting claim does not clearly set forth the metes and bounds of the patent protection desired.

Same rejection's reason for claim 30, line 2.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 5, 9-11, 13-17, 19, 23-25, 27-29, 31, 33, 37-39, and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Platko et al.** (U.S.6,363,444) in view of **Chan et al.** (U.S.4,969,121).

- In regard to claims 1, 15 and 29, **Platko** discloses in Figs. 1-7 and in the respective portions of the specification about the processing systems used in host systems ("*host system*")

such as personal computers and workstations; where the master/slave processors are embedded in the network interface card 'NIC' with complex 'ASIC' logic ("*application specific integrated circuit*") and coupled to the memory via the memory data bus for controlling the reading, writing and transferring data among different processing elements (For example see Fig. 1; Abstract; col. 1, lines 21-50); wherein the NIC card comprises the processor 28 in the ASIC 16 connected to the electrically erasable programmable read only memory 26 'EEPROM' ("*programmable logic core*"); the media access control ("*MAC*") logic 44 for interfacing the ASIC 16 ("*first portion*") to the external PHY logic 24 ("*network interface subsystem*"; For example see Fig. 1) and processing control data (For example see col. 1, lines 35-50; col. 2, lines 17-30) via the DMA control logic (For example see col. 3, lines 46-49; col. 7, lines 44-48); and the PCI interface logic 42 for interfacing the ASIC 16 ("*second portion*") to the external PCI bus 12 ("*data transmission subsystem*") via the PCI interface logic 42 and transmitting/receiving data stored in the SRAM ("*memory device*") in response to the host (For example see col. 4, lines 1-5; col. 5, line60 through col. 6, line 2). **Platko** does disclose about the programmable logic with the electrically erasable programmable read only memory 'EEPROM', but fails to explicitly disclose "*array of configurable arithmetic logic units*". However, such implementation is known in the art.

For example, **Chan** discloses in Figs. 1-4 and in the respective portions of the specification about the programmable integrated circuit logic array device using the EEPROM array ("*array of configurable arithmetic logic units*"; For example see Figs. 1-4; Abstract; col. 2, lines 47-55; col. 11, line 65 through col. 12, line 20); which can be programmed to perform various logic functions.

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Chan**, by implementing the EEPROM array into the **Platko**'s EEPROM, with the motivation being to improve the ability in performing more logic functions and being programmable to a greater degree as disclosed in **Chan**: col. 1, lines 41-45.

- Regarding claim 16, the combination of **Platko** and **Chan** further discloses about the left and right macrocells ("*first and second portions*") with the EEPROM logic array ("*programmable logic cores*"; For example see **Chan**: Figs. 1-3; col. 2, lines 33-55).

Thus it would have been obvious to the person of ordinary skill in the art at the time of the invention was made to combine the invention as taught by **Chan**, by implementing the EEPROM array into the **Platko**'s EEPROM, with the motivation being to improve the ability in performing more logic functions and being programmable to a greater degree as disclosed in **Chan**: col. 1, lines 41-45.

- In regard to claims 3, 17 and 31, the combination of **Platko** and **Chan** further discloses about the transferring control and data through the processor 28 ("*programmable logic core*"; For example see **Platko**: Fig. 1; col. 5, line 55 through col. 6, line 2) under the control of the host system disclosed in **Platko**: col. 4, lines 1-5.

- Regarding claims 5, 9, 19, 23, 33 and 37, the combination of **Platko** and **Chan** further discloses about the master and slave devices ("*master and slave devices*"; For example see

Platko: Fig. 1; Abstract; col. 3, lines 61-67) in transferring data over the internal/external bus ("*master and slave bus*"; For example see **Platko**: Fig. 1; col. 3, lines 34-42; col. 8, lines 47-48).

- In regard to claims 10-11, 24-25 and 38-39, the combination of **Platko** and **Chan** further discloses about the DMA engines and datapath control logic are programmed for transferring control and data among the PCI interface logic, PCI bus, MAC, memory control and T Bus ("*DMA controller, data bus, control bus*"; For example see **Platko**: Fig. 1; col. 3, lines 46-49; col. 5, line 60 through col. 6, line 2).

- Regarding to claims 13, 27 and 41, the combination of **Platko** and **Chan** further discloses about the FIFO buffer ("*first-in-first-out buffer*") with data RAM 34 and instruction RAM 32 (For example see **Platko**: Figs. 1, 4; col. 7, lines 9-24).

- In regard to claims 14, 28 and 42, the combination of **Platko** and **Chan** further discloses about the network interface for connecting the system to the Ethernet network and controlling transmitted/received packet to/from the Ethernet ("ethernet controller"; For example see Fig. 1; col. 3, lines 14-18; col. 4, lines 26-46).

Allowable Subject Matter

7. Claims 6, 20-21 and 34-35 would be allowable if rewritten or amended to overcome the objection set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 4, 7-8, 12, 18, 22, 26, 32, 36 and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chang (U.S.6,260,087), **Cromer et al.** (U.S.6,263,388), **Vaidar, Theodore** ("PLC advanced technology demonstrator TestChipB", LSI Logic Corp, May 2001, IEEE, 0-7803-6591, pages 67-70), **Wilton et al.** ("Programmable Logic IP Cores in SoC Design: Opportunities and Challenges", University of British Columbia, Canada, IEEE, 0-7803-6591, pages 63-66) and **Hallschmid et al.** ("Detailed Routing Architectures for Embedded Programmable Logic IP Cores", Department of Electrical and Computer Engineering, University of British Columbia, Canada, February 2001, pages 69-74) are all cited to show devices and methods for improving the program logic of the ASIC in the communication architectures, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (571) 272-3074. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRIAN NGUYEN
PRIMARY EXAMINER

Tri H. Phan
January 19, 2005